What is claim is:

1. A test structure for determining process misalignment during manufacturing of an integrated circuit, comprising:

a first conductive layer having a first finger-shaped structure and a second finger-shaped structure;

a dielectric layer formed on the first conductive layer; and

a second conductive layer formed on the dielectric layer, the second conductive layer having a third finger-shaped structure and a fourth finger-shaped structure corresponding to the first finger-shaped structure and the second finger-shaped structure respectively;

wherein the third finger-shaped structure partially overlaps the first finger-shaped structure by an predetermined overlap width (W) in a first direction, and the fourth finger-shaped structure partially overlaps the second finger-shaped structure by the predetermined overlap width in a second direction, and wherein the first direction is opposite to the second direction.

2. The test structure of claim 1, wherein the first conductive layer further comprises a plurality of the first finger-shaped structures and a plurality of the second finger-shaped structures, and wherein the second conductive layer further comprises a plurality of the third finger-shaped structures and a plurality of the fourth finger-shaped structures corresponding to the first finger-shaped structures and the second finger-shaped structures respectively.

3. The test structure of claim 1, wherein misalignment induced in a process of forming the second conductive layer causes an offset amount of the third finger-shaped structure and the fourth finger-shaped structure such that the third and the fourth finger-shaped structures respectively overlap the first and the second finger-shaped

structures by a first overlap width and a second overlap width.

4. The test structure of claim 3, wherein the first overlap width equals the predetermined overlap width minus the offset amount, and the second overlap width equals the predetermined overlap width plus the offset amount while the misalignment occurs in the first direction.

5. The test structure of claim 3, wherein the first overlap width equals the predetermined overlap width plus the offset amount, and the second overlap width equals the predetermined overlap width minus the offset amount while the misalignment occurs in the second direction.

6. The test structure of claim 4 or claim 5, wherein the offset amount is calculated by measuring an electrical characteristic across the first conductive layer and the second conductive layer.

7. The test structure of claim 1, wherein the first finger-shaped structure overlaps the third finger-shaped structure by a first overlap length (L1) and the second finger-shaped structure overlaps the fourth finger-shaped structure by a second overlap length (L2), and wherein the L1 and the L2 are much larger than the W respectively.

8. The test structure of claim 7, wherein the first overlap length (L1) and the second overlap length (L2) are equal to an overlap length (L).

9. The test structure of claim 8, wherein an offset amount (W') resulting from the misalignment is calculated from the equation W'=W*(C1-C2)/(C1+C2), wherein W is the predetermined overlap width; C1 and C2 are a first capacitance and a second capacitance respectively created due to the overlap between the first and the third finger-shaped structures and the overlap between the second and the fourth finger-shaped structures.

10. The test structure of claim 9, wherein

while the W' is larger than zero, the second conductive layer shifts to the second direction during a patterning process;

while the W' is less than zero, the second conductive layer shifts to the first direction during a patterning process; and

while the W' equals zero, the second conductive layer doesn't shift during a patterning process.

11. The test structure of claim 8, wherein an offset amount (W') resulting from the misalignment is calculated from the equation W'=W*(C2-C1)/(C1+C2), wherein W is the predetermined overlap width; C1 and C2 are a first capacitance and a second capacitance respectively created due to the overlap between the first and the third finger-shaped structures and by the overlap between the second and the fourth finger-shaped structures.

12. The test structure of claim 11, wherein

while the W' is larger than zero, the second conductive layer shifts to the first direction during a patterning process;

while the W' is less than zero, the second conductive layer shifts to the second direction during a patterning process; and

while the W' equals zero, the second conductive layer doesn't shift during a patterning process.

13. A method of determining process misalignment during manufacturing of an integrated circuit having a first conductive layer, the method comprising:

patterning the first conductive layer to form a first finger-shaped structure and a second finger-shaped structure;

forming a dielectric layer on the first conductive layer;

forming a second conductive layer on the dielectric layer;

patterning the second conductive layer to form a third finger-shaped structure and a fourth finger-shaped structure respectively partially overlapping the first finger-shaped structure in a first direction and the second finger-shaped structure in a second direction by a predetermined overlap width (W), the first direction being opposite to the second direction;

measuring an electrical characteristic across the first conductive layer and the second conductive layer to determine whether the second conductive layer is shifted during a patterning process.

14. The method of claim 13, wherein the step of patterning the first conductive layer further comprises forming a plurality of the first finger-shaped structures and a plurality of the second finger-shaped structures.

15. The method of claim 14, wherein the step of patterning the second conductive layer further comprises patterning the second conductive layer to form a plurality of the third finger-shaped structures and a plurality of the fourth finger-shaped structures respectively partially overlapping the first finger-shaped structures in said first direction and the second finger-shaped structures in said second direction by the predetermined overlap width.

16. The method of claim 13, wherein the step of patterning the second conductive layer further comprises forming the third and the fourth finger-shaped structures to respectively overlap the first and the second finger-shaped structures by an identical overlap length (L), and wherein the L is much larger than the W.

17. The method of claim 16, wherein the step of determining whether the second conductive layer is shifted comprises calculating an offset amount (W') of the patterned second conductive layer from the equation W'=W*(C1-C2)/(C1+C2),

wherein W is the predetermined overlap width; C1 and C2 is a first capacitance and a second capacitance respectively created due to the overlap between the first and the third finger-shaped structures and the overlap between the second and the fourth finger-shaped structures.

18. The method of claim 17, wherein

while the W' is larger than zero, the second conductive layer shifts to the second direction during a patterning process;

while the W' is less than zero, the second conductive layer shifts to the first direction during a patterning process; and

while the W' equals zero, the second conductive layer doesn't shift during a patterning process.

19. The method of claim 16, wherein the step of determining whether the second conductive layer is shifted comprises calculating an offset amount (W') of the patterned second conductive layer from the equation W'=W*(C2-C1)/(C1+C2), wherein W is the predetermined overlap width; C1 and C2 are a first capacitance and a second capacitance respectively created due to the overlap between the first and the third finger-shaped structures and the overlap between the second and the fourth finger-shaped structures.

20. The method of claim 19, wherein

while the W' is larger than zero, the second conductive layer shifts to the first direction during a patterning process;

while the W' is less than zero, the second conductive layer shifts to the second direction during a patterning process; and

while the W' equals zero, the second conductive layer doesn't shift during a patterning process.